**Сводный отчет использования ресурсов микросхемы Spartan6 при моделировании нейросети Джордана**

**Дискретная модель сети Джордана (4 входа, 8 нейронов, 9 бит/коэффициент)**

Primitive and Black Box Usage:

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# BELS : 2482

# GND : 1

# LUT2 : 66

# LUT3 : 407

# LUT4 : 585

# LUT5 : 8

# LUT6 : 40

# MUXCY : 640

# MUXF7 : 14

# VCC : 1

# XORCY : 720

# FlipFlops/Latches : 13

# FD : 2

# FDE : 11

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 442

# IBUF : 437

# OBUF : 5

Device utilization summary:

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Selected Device : 6slx16ftg256-3

Slice Logic Utilization:

Number of Slice Registers: 13

Number of Slice LUTs: 1106

Number used as Logic: 1106

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 1112

Number with an unused Flip Flop: 1099

Number with an unused LUT: 6

Number of fully used LUT-FF pairs: 7

Number of unique control sets: 4

IO Utilization:

Number of IOs: 443

Number of bonded IOBs: 443

Minimum period: 18.001ns (Maximum Frequency: 55.553MHz)

Minimum input arrival time before clock: 18.791ns

Maximum output required time after clock: 21.152ns

Maximum combinational path delay: 21.943ns

**Непрерывная модель сети Джордана (4 входа, 8 нейронов, 32 бит/коэффициент)**

Primitive and Black Box Usage:

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# BELS : 9065

# GND : 1

# LUT2 : 250

# LUT3 : 1560

# LUT4 : 2094

# LUT5 : 9

# LUT6 : 51

# MUXCY : 2539

# VCC : 1

# XORCY : 2560

# FlipFlops/Latches : 11

# FD : 2

# FDE : 9

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 1546

# IBUF : 1541

# OBUF : 5

Device utilization summary:

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Selected Device : 6slx16ftg256-3

Slice Logic Utilization:

Number of Slice Registers: 11

Number of Slice LUTs: 3964

Number used as Logic: 3964

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 3971

Number with an unused Flip Flop: 3960

Number with an unused LUT: 7

Number of fully used LUT-FF pairs: 4

Number of unique control sets: 4

IO Utilization:

Number of IOs: 1547

Number of bonded IOBs: 1547

Minimum period: 21.695ns (Maximum Frequency: 46.093MHz)

Minimum input arrival time before clock: 21.237ns

Maximum output required time after clock: 24.780ns

Maximum combinational path delay: 24.322ns